**TITLE: MICROPROCESSOR BASED SYSTEM**

**Last task#7**



**Spring 2023**

**THEORY CSE307 MBSD**

Submitted by:

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“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

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Submitted to:

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(Wednesday, 11may, 2023)

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Generator

8

Sine

Wave

ADC

0804

Oscilloscope

|  |  |  |
| --- | --- | --- |
| 89C51  MCU-2 8 | DAC  0808 | |
|  | |  |

89C51

MCU-1

Figure 1: Block diagram of all the components Design the following two cases A and B, and then answer questions in C.

1. Frequency of input sine wave (**f\_in**) is **30**Hz.
   1. Sampling rate (**fs)** of ADC = **300** samples/sec.
   2. Transmission rate of serial data is **9600** bps between MCU-1 and MCU-2.
   3. Oscillator frequency = 11.059MHz.
2. If oscillator frequency is fixed at 22.118MHz for both microcontrollers. Keeping in view the *fastest possible transmission* rate of serial communication and *ADC conversion rate*. How much the frequency of input signal can be increased? Run the system at that frequency in Proteus.
3. Discuss,

Input signal to ADC has a frequency (**f\_in)** of 30Hz. How you supplied it

Ans:

To supply a 30Hz input signal to the ADC:

Use a signal generator or microcontroller to generate a 30Hz sine wave and connect its output to the ADC input.

Ensure proper voltage levels and signal conditioning for the ADC input, considering voltage range, impedance, and anti-aliasing filtering if needed.

* What happens if you decrease the sampling rate (**fs**) from 300Hz to 60Hz samples per second for ADC?

Ans:

if the sampling rate (fs) of the ADC is decreased from 300Hz to 60Hz:

The maximum accurately representable frequency would decrease from 150Hz to 30Hz according to the Nyquist-Shannon sampling theorem.

Decreasing the sampling rate too much can result in the loss of high-frequency components, aliasing, and distortion in the sampled data, affecting the fidelity and accuracy of the digitized signal.

* What reference voltage (V\_ref) has been used for ADC?

I used a 𝑉𝑟𝑒𝑓 = 1.02 because this provided me with a range 0 to 2.04V and 255/2.04 = 0.008

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which is an exact float that is easy to work with.

* What is the relationship of **V\_ref** to the amplitude of input signal?

The range of input to ADC must be withing 0 to Vref so in case of sine wave, the amplitude should be half of Vref (not Vref/2) and the offset should be same as amplitude so that the signal lies between 0 to Vref and does not go into negative.

The reference voltage (V\_ref) establishes the maximum voltage range that the ADC can represent. The amplitude of the input signal should not exceed the reference voltage range to ensure accurate conversion of the signal into digital values.

* What will be the step-size?

Since my Dynamic range is (0 to 2.04) the step size is = 0.008.

* What is the input voltage range of ADC ?

1. to 2.04V

* Can we increase the frequency of input signal (**f\_in)** to 10KHz, if not then why? • If transmission rate is increased to 19,200 bps. Is your design able to handle input frequency (f\_in) equal to 10KHz, without any loss of information? Assuming **fs** = = 10 x **f\_in**. • What is the limit of DAC, how fast it can work?

The maximum transmission rate we can get is 57.6 Khz (by setting SMOD to 1 and TH1 = 0xff). While it is possible to transmit a signal sampled at 10Khz with a transmission rete of 57.6 Khz, it does violate the condition given in question.

If we increate transmission rate to 19200 bps means 1920 bytes per second and it cannot handle 10 K bytes per second. In my code, a lot of packets will get dropped.

DAC has diodes and resistors, and these components don’t have any delays associated with so DAC’s

output is generated instantaneously in almost real time.

Code: